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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,713	04/14/2004	Jae-Bon Koo	6161.0123.US	5231

7590 05/05/2005

McGuire Woods LLP
Suite 1800
1750 Tysons Boulevard
McLean, VA 22102

EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,713	KOO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 1405*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *5,7-10,13-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Embodiment 1 (Fig. 3A-3B, claims 1-4, 6, 11, and 12) in the reply filed on 4/14/2003 is acknowledged. The traversal is on the ground(s) that the subject matter of all claims is sufficiently related that a thorough search of any one species would encompass a search that the subject matter of the remaining species. This is not found persuasive because embodiments 2-7 comprise at least one offset region(s) including undoped region, a gate with certain width/length dimension and/or geometrical structure, while embodiment 1 comprises none of these features.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. The drawings are objected to because the bottom left corner of fig. 7A has not been labeled and it is not clear whether it is part of the drawing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be

labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference numerals 661, 665 and 321 are not shown in figs. 6 and 7. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. Claim 3 is objected to because of the following informalities: The recitation "a thin film resistor ..." should read "a thin film transistor ...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohtani ("Ohtani") EP 1033755.

Ohtani discloses (figs. 1-14 and col. 7, lines 5-45) a flat panel display, comprising: a pixel array portion 1001 having a plurality of pixels arranged thereon; and a driving circuit portion 1002/1003 for driving the plurality of pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion has a different resistance value than a thin film transistor in the driving circuit portion.

Regarding claim 2, Ohtani discloses the pixel array portion and the driving circuit portion each having a plurality of thin film transistors and where at least one thin film transistor of the plurality of thin film transistors in the pixel array portion has a resistance value higher than any of the plurality of thin film transistors in the driving circuit portion.

6. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. ("Yamazaki") USPN 5,858,823.

Yamazaki discloses (figs. 10-11 and col. 17, lines 11-58) a flat panel display, comprising: a pixel array portion 3 having a plurality of pixels arranged thereon; and a driving circuit portion 1/2 for driving the plurality of pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion has a different resistance value than a thin film transistor in the driving circuit portion.

Regarding claim 2, Yamazaki discloses the pixel array portion and the driving circuit portion each having a plurality of thin film transistors and where at least one thin film transistor of the plurality of thin film transistors in the pixel array portion has a resistance value higher than any of the plurality of thin film transistors in the driving circuit portion.

7. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. ("Lin") US PG-Pub 2004/0096999.

Lin discloses (figs. 9-16 and pars. 0036 and 0038) a flat panel display, comprising: a pixel array portion 101 having a plurality of pixels arranged thereon; and a driving circuit portion 103 for driving the plurality of pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion has a different resistance value than a thin film transistor in the driving circuit portion.

Regarding claim 2, Lin discloses the pixel array portion and the driving circuit portion each having a plurality of thin film transistors and where at least one thin film transistor of the plurality of thin film transistors in the pixel array portion has a resistance value higher than any of the plurality of thin film transistors in the driving circuit portion.

8. Claims 3, 4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohtani.

Ohtani discloses (figs. 1-14 and col. 7, lines 5-45) a flat panel display, comprising: a pixel array portion 1001 having a plurality of pixels arranged thereon; and a driving circuit portion 1002/1003 for driving the plurality pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion has a different resistance value in its gate region than a thin film resistor in the driving circuit portion.

Regarding claim 4, Ohtani discloses one thin film transistor of the thin film transistor in the pixel array portion and the thin film transistor in the driving circuit portion including an offset region in its gate region 106/113.

Regarding claim 6, Ohtani discloses the thin film transistor in the pixel array portion includes an offset region 113 in its gate region.

9. Claims 3, 4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin.

Lin discloses (figs. 9-16 and pars. 0036 and 0038) a flat panel display, comprising: a pixel array portion 101 having a plurality of pixels arranged thereon; and a driving circuit portion 103 for driving the plurality pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion has a different resistance value in its gate region than a thin film resistor in the driving circuit portion.

Regarding claim 4, Lin discloses one thin film transistor of the thin film transistor in the pixel array portion and the thin film transistor in the driving circuit portion including an offset region in its gate region 148.

Regarding claim 6, Lin discloses at the thin film transistor in the pixel array portion includes an offset region 148 in its gate region.

10. Claims 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohtani.

Ohtani discloses (figs. 1-14 and col. 7, lines 5-45) a flat panel display, comprising: a pixel array portion 1001 having a plurality of pixels arranged thereon; and a gate driving circuit portion 1002 and a data driving circuit portion 1003 for driving the plurality of pixels of the pixel array portion, wherein at least one thin film transistor of a plurality of thin film transistors in the pixel array portion has a different resistance value from at least one thin film transistor of a

plurality of thin film transistors in the gate driving circuit portion and the data driving circuit portion.

Regarding claim 12, Ohtani discloses the at least one thin film transistor of the plurality of thin film transistors in the pixel array portion including an offset region 113 in its gate region.

11. Claims 3, 4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin.

Lin discloses (figs. 9-16 and pars. 0036 and 0038) a flat panel display, comprising: a pixel array portion 101 having a plurality of pixels arranged thereon; and a gate driving circuit portion 103 and a data driving circuit portion 103 for driving the plurality of pixels of the pixel array portion, wherein at least one thin film transistor of a plurality of thin film transistors in the pixel array portion has a different resistance value from at least one thin film transistor of a plurality of thin film transistors in the gate driving circuit portion and the data driving circuit portion.

Regarding claim 12, Lin discloses the at least one thin film transistor of the plurality of thin film transistors in the pixel array portion including an offset region 148 in its gate region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
April 26, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800